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10/813,060	03/31/2004	Alexander R. LaChance	9-14774-13US	4650

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EXAMINER	
PARK, EDWARD	
ART UNIT	PAPER NUMBER
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/813,060	LACHANCE ET AL.	
	Examiner	Art Unit	
	EDWARD PARK	2624	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *31 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. This action is responsive to applicant's amendment and remarks received on 2/5/08. Claims 1-17 are currently pending.

Claim Rejections - 35 USC § 101

2. In response to applicant's cancellation of claims 18 and 20, the previous claim rejections are withdrawn.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. **Claims 1, 11, 12, 13, 14, 15, 17** are rejected under 35 U.S.C. 103(a) as being unpatentable over Abt et al (US 2003/0084409 A1) in view of Jouandet (US 5,038,285).

Regarding **claims 1, 11, 12**, Abt teaches a method for producing a three-dimensional model of a semiconductor chip from coarsely aligned mosaic images of respective layers of the

semiconductor chip (figure 1), the method comprising: applying a line detection algorithm to each of the mosaic images (Abt: figure 1, numeral 12, 13); and processing to define vias, lines and branch lines of the semiconductor chip, interconnected to define the three-dimensional model (Abt: figure 1, numeral 17, paragraph [0048]). Abt does not teach producing a set of line segments identified by x and y coordinates of ends of each line segment with respect to a frame defined by the mosaic image; establishing virtual reference marks using end points of different mosaic images that are vertically aligned to within an uncertainty of the coarse alignment of the mosaic images; using the virtual reference marks to adjust x and y coordinates of each of the mosaic images to derive a three dimensional coordinate space; processing the end points within the three dimensional coordinate space; counting a number of other mosaic images that have coincident end points in a common projective x-y plane within an uncertainty of the coarse layer alignment; identifying end points with a high coincidence in the x-y plane; selecting from the identified end points the virtual reference marks; and identifying a mosaic image having end points associated with a highest percentage of the virtual reference marks, and aligning each mosaic image to the identified mosaic image by adjusting x and y coordinates of each of the other mosaic images.

Jouandet teaches producing a set of line segments identified by x and y coordinates of ends of each line segment with respect to a frame defined by the mosaic image (Jouandet: figure 1, numeral 20); establishing virtual reference marks using end points of different mosaic images that are vertically aligned to within an uncertainty of the coarse alignment of the mosaic images (Jouandet: figure 1, numeral 22); using the virtual reference marks to adjust x and y coordinates of each of the mosaic images to derive a three dimensional coordinate space (Jouandet: figure 2,

numeral 26); processing the end points within the three dimensional coordinate space (Jouandet: figure 3); counting a number of other mosaic images that have coincident end points in a common projective x-y plane within an uncertainty of the coarse layer alignment (Jouandet: figure 2, numeral 32); identifying end points with a high coincidence in the x-y plane (Jouandet figure 2, numeral 32); selecting from the identified end points the virtual reference marks (Jouandet figure 2, numeral 32); and identifying a mosaic image having end points associated with a highest percentage of the virtual reference marks (Jouandet figure 2, numeral 32), and aligning each mosaic image to the identified mosaic image by adjusting x and y coordinates of each of the other mosaic images (Jouandet: figure 3).

It would have been obvious at the time the invention was made to one of ordinary skill in the art to modify the Abt reference to identify line segments, establish virtual reference marks, adjust coordinates, process the end points, identify end points with high coincidence, and align each mosaic image as suggested by Jouandet, to "produc[e] two-dimensional maps of three-dimensional surfaces" (Jouandet: col. 1, lines 8-9) that "reduc[es] distortion between straight lines representations" (Jouandet: col. 3, lines 13-16).

Regarding **claim 13**, Abt teaches wherein processing the end points further comprises using predefined rules regarding configuration of the line segments to define lines and branch lines of the semiconductor chip (Abt: paragraph [0043]).

Regarding **claims 14, 15, 17**, Abt with Jouandet combination discloses all elements as mentioned above in claim 1. Abt with Jouandet combination as mentioned above does not teach displaying the 3-dimensional model to an operator, as a set of lines of predefined thickness.

Jouandet further teaches displaying the 3-dimesional model to an operator, as a set of lines of predefined thickness (Jouandet: figure 4, numeral 76), permitting the user to view any one of the mosaic images alone, the mosaic images with the 3-D model overlayed, and the 3-D model alone (Jouandet: figure 4, numeral 76); and permitting the operator to select a geometric area and displaying a part of the 3-D model in the geometric area (Jouandet: figure 4).

It would have been obvious at the time the invention was made to one of ordinary skill in the art to modify the Abt with Jouandet combination to display a 3-dimensional model to an operator as suggested by Jouandet, to allow the user to visualize the object; allow the user to alter any parameters; or observe any defects that may have not been detected and corrected.

5. **Claims 2, 3, 4, 5, 6, 9, and 10** are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Abt et al (US 2003/0084409 A1) with Jouandet (US 5,038,285) as applied to claim 1 above with Companion et al (US 6,330,354 B1), and further in view of Maruyama (US 5,272,763).

Regarding **claims 2, 3, 4, 5, 6, 9, and 10** Abt with Jouandet combination discloses all elements as mentioned above in claim 1. Abt with Jouandet combination does not teach:

applying an edge detector to obtain an edge bitmap defining edge objects;

selecting pixel regions of edge objects that are likely to constitute segments of metal lines, given parameters of the semiconductor chip;

applying a line tracing algorithm to each edge object to identify and store coordinates of corresponding line segments;

storing line segment coordinates in a hierarchical format with branch line segments nested with respect to previously identified line segments;

applying an algorithm that computes a difference between pixel values of neighboring pixels on opposite sides of a subject pixel to determine that the subject pixel is an edge transition pixel if the difference is above a predefined threshold;

applying an algorithm derived from at least one of Sobel, Prewitt, Roberts, and Hough transforms;

applying a line thinning procedure to pixels of the mosaic image bounded by the pixel regions of selected edge objects to produce a thinned line;

defining the line segments by coordinate positions of the pixels at the ends of line segments, and storing the end point coordinates in a database;

computing for each line segment a measure of uncertainty that the line segment constitutes a part of a metal line, using properties of the edge object, and properties of the thinned line give the die properties; and

requesting an operator to examine the line segments with uncertainty measures above a predefined threshold.

Companion teaches:

applying an edge detector to obtain an edge bitmap defining edge objects (Companion: figure 2b, numeral 120);

selecting pixel regions of edge objects that are likely to constitute segments of metal lines, given parameters of the semiconductor chip (Companion: figure 2b, numeral 120);

applying an algorithm that computes a difference between pixel values of neighboring pixels on opposite sides of a subject pixel to determine that the subject pixel is an edge transition pixel if the difference is above a predefined threshold (Companion col. 5, lines 1-21);

applying an algorithm derived from at least one of Sobel, Prewitt, Roberts, and Hough transforms (Companion: col. 5, lines 1-21); and

computing for each line segment a measure of uncertainty that the line segment constitutes a part of a metal line, using properties of the edge object, and properties of the thinned line give the die properties (Companion: figure 2b, numeral 124, 126).

requesting an operator to examine the line segments with uncertainty measures above a predefined threshold (Companion: figure 2b, numeral 140).

It would have been obvious at the time the invention was made to one of ordinary skill in the art to modify the Abt with Jouandet combination to apply an edge detector, select pixel regions, apply a Hough transform as suggested by Companion, to rule out "false positives [that] would most likely occur [but are difficult] to handle [within many] layers, [of] repetitive pattern sequences" (Companion: col. 1, lines 55-65).

Maruyama teaches:

applying a line tracing algorithm to each edge object to identify and store coordinates of corresponding line segments (Maruyama: col. 9, lines 59-68; col. 10, lines 1-23);

storing line segment coordinates in a hierarchical format with branch line segments nested with respect to previously identified line segments (Maruyama: col. 3, lines 1-28);

applying a line thinning procedure to pixels of the mosaic image bounded by the pixel regions of selected edge objects to produce a thinned line (Maruyama: col. 9, lines 59-68; col. 10, lines 1-23); and

defining the line segments by coordinate positions of the pixels at the ends of line segments, and storing the end point coordinates in a database (Maruyama: col. 9, lines 59-68; col. 10, lines 1-23).

It would have been obvious at the time the invention was made to one of ordinary skill in the art to modify the Abt, Jouandet, with Companion combination as mentioned above to apply a line tracing algorithm, storing in a hierarchical format, line thinning procedure, and coordinate positions of the pixels as suggested by Maruyama, to "accurately perform the wiring pattern inspection without requiring complex positioning" which is essential due to the numerous lines that are present.

6. **Claims 7, 8** are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Abt et al (US 2003/0084409 A1), Jouandet (US 5,038,285), Companion et al (US 6,330,354 B1), with Maruyama (US 5,272,763) as applied to claim 6 above, and further in view of Martin et al (Robotics, "Image Processing Techniques for Machine Vision").

Regarding **claims 7 and 8**, Abt, Jouandet, Companion, with Maruyama combination discloses all elements as mentioned above in claim 6. Abt, Jouandet, Companion, with Maruyama combination does not teach iteratively setting pixel values of boundary pixels to a background pixel value, until the pixels that remain are bounded by background pixel values on two sides and applying an algorithm derived from at least one of a Zhang Suen skeletonizing algorithm, and a Stentiford skeletonizing algorithm.

Martin teaches iteratively setting pixel values of boundary pixels to a background pixel value, until the pixels that remain are bounded by background pixel values on two sides (Martin:

pg. 6, right column) and applying an algorithm derived from at least one of a Zhang Suen skeletonizing algorithm, and a Stentiford skeletonizing algorithm (Martin: pg. 6-8).

It would have been obvious at the time the invention was made to one of ordinary skill in the art to modify the Abt, Jouandet, Companion, with Maruyama combination to utilize a Stentiford skeletonizing algorithm as suggested by Martin, to "erode the outer layers of pixel until no more layers can be removed" which proves to be a "popular because of their reliability and effectiveness" (Martin: pg. 7, left column).

7. **Claim 16** is rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Abt et al (US 2003/0084409 A1) with Jouandet (US 5,038,285) as applied to claim 14 above, and further in view of Phan et al (US 6,808,591 B1).

Regarding **claim 16**, Abt with Jouandet discloses all elements as mentioned above in claim 14. Abt with Jouandet combination does not teach permitting the operator to select any line, to create an annotation for a selected line; and to edit the connectivity of the line segments, and placements of vias.

Phan teaches permitting the operator to select any line, to create an annotation for a selected line; and to edit the connectivity of the line segments, and placements (Phan: col. 4, lines 15-35).

It would have been obvious at the time the invention was made to one of ordinary skill in the art to modify the Abt with Jouandet combination to allow the operator to select and edit line segments and placements as suggested by Phan, to further enhance the operator's ability to examine and rectify any defective line segments by graphical analysis.

Response to Arguments

8. Applicant's arguments filed on 2/5/08, in regards to **claim 1**, have been fully considered but they are not persuasive. Applicant argues that Abt reference does not produce a "three-dimensional model of a semiconductor chip". This argument is not considered persuasive since in paragraph [0048], it states that "images of the system work together to represent the original three-dimensional layout of metal, polysilicon, and inter-connective layers", which is equivalent to a three-dimensional model of a semiconductor chip.

Applicant continues to argue that the secondary reference Jouandet is not analogous prior art and therefore can not be combined with the Abt reference in a rejection under 35 U.S.C. 103. In response to applicant's argument that Jouandet is nonanalogous art, it has been held that a prior art reference must either be in the field of applicant's endeavor or, if not, then be reasonably pertinent to the particular problem with which the applicant was concerned, in order to be relied upon as a basis for rejection of the claimed invention. See *In re Oetiker*, 977 F.2d 1443, 24 USPQ2d 1443 (Fed. Cir. 1992). In this case, Jouandet is reasonably pertinent in resolving the claim limitations of claim 1. Applicant argues that Jouandet teaches a method "for deriving a planar representation of a three-dimensional surface". This argument is not considered persuasive since it is irrelevant what the overall invention intends to do, but rather Jouandet's inventive concepts within the invention is what is used to combine with Abt reference. Applicant argues that Jouandet does not teach "a method for producing a three-dimensional model of a semi conductor chip. This argument is not considered persuasive since the primary reference discloses that particular claim limitation which is the preamble. In response to applicant's arguments against the references individually, one cannot show nonobviousness by

attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.,* 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). In response to applicant's arguments, the recitation "a method for producing a three-dimensional model of a semi conductor chip" has not been given patentable weight because the recitation occurs in the preamble. A preamble is generally not accorded any patentable weight where it merely recites the purpose of a process or the intended use of a structure, and where the body of the claim does not depend on the preamble for completeness but, instead, the process steps or structural limitations are able to stand alone. See *In re Hirao*, 535 F.2d 67, 190 USPQ 15 (CCPA 1976) and *Kropa v. Robie*, 187 F.2d 150, 152, 88 USPQ 478, 481 (CCPA 1951).

In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.,* 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

In response to applicant's argument that applicant's reasons for solving the problem of how to achieve accurate vertical alignment between discontinuous structures in coarsely aligned mosaic images, the fact that applicant has recognized another advantage which would flow naturally from following the suggestion of the prior art cannot be the basis for patentability when the differences would otherwise be obvious. See *Ex parte Obiaya*, 227 USPQ 58, 60 (Bd. Pat. App. & Inter. 1985).

In response to applicant's arguments that the secondary reference Jouandet does not teach "establishing virtual reference marks …… to define the three-dimensional model", is not

considered persuasive since the limitations and motivation are explained above. Examiner notes that the primary reference discloses applying a line detection algorithm to each of the mosaic images; and processing to define vias, lines and branch lines of the semiconductor chip, interconnected to define the three-dimensional model. The secondary teaches the remaining limitations of claim 1 which is basically identifying virtual reference marks which are in 2 dimensions and aligning to create a three-dimensional model through compiling frames vertically.

Furthermore, the applicant argues that the Jouandet reference disclose reference points that do not relate to endpoints in different mosaic images. This argument is not considered persuasive since the limitations are taught in the reference and explained above in the rejection and arguments.

Conclusion

9. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event,

however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to EDWARD PARK whose telephone number is (571)270-1576. The examiner can normally be reached on M-F 10:30 - 20:00, (EST).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Vikkram Bali can be reached on (571) 272-7415. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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